UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,243	07/03/2003	Yen-Yu Lin	MTKP0009USA	1242

27765 7590 01/09/2007

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
MILLER, BRANDON J	
ART UNIT	**PAPER NUMBER**
2617	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/604,243	LIN, YEN-YU	
	Examiner	Art Unit	
	Brandon J. Miller	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Settle et al. (US 6,233,253 B1) in view of Hong et al. (US 7,106,757 B2).

Regarding claim 1 Settle teaches a transmission circuit that receives input data at a first rate and outputs data at a second rate (see col. 8, lines 41-44). Settle teaches a processor for controlling operations of the transmission circuit, the processor capable of accepting input data and generating corresponding first data having a plurality of bits (see col. 8, lines 41-50 and col. 13, lines 37-41). Settle teaches a format converting circuit electrically connected to the processor for generating second data having a plurality of bits according to the first data (see col. 8, lines 41-50). Settle teaches a plurality of input units each for receiving on bit of the first data and a plurality of output units each for outputting one bit of the second data after receiving the bit (see col. 8, lines 39-44 and FIG. 7). Settle teaches a bit control circuit electrically connected between the input units and the output units for generating bits outputted by the output units according to bits received from the input units (see col. 8, lines 41-50, col. 13, lines 37-41, and FIG. 7). Settle teaches transmitting a bit received by an input unit to an output unit without having the bit passing through other input and output units (see col. 8, lines 39-44). Settle teaches wherein the processor further controls the transmission circuit to output data sequentially

according to the second data (see col. 5, lines 27-30). Settle does not specifically teach a number of bits between the bit received by the input unit and a most significant bit of the first data being different from a number of bits between the bit outputted by the output unit and a most significant bit of the second data. Hong teaches a number of bits between the bit received by the input unit and a most significant bit of the first data being different from a number of bits between the bit outputted by the output unit and a most significant bit of the second data (see col. 4, lines 26-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device adapt to include a number of bits between the bit received by the input unit and a most significant bit of the first data being different from a number of bits between the bit outputted by the output unit and a most significant bit of the second data because it would allow for Settle to achieve improved output quality in his system that converts data from different input sources and different formats to form a bit-stream for output in a selected output format.

Regarding claim 2 Settle teaches a processor that is capable of buffering the first or second data so that the processor outputs data at a second rate according to the second data (see col. 4, lines 6-11).

Regarding claim 3 Settle teaches an operating circuit electrically connected between the input units and the output units for performing a logical operation according to predetermined law on the bits received by the input units to generate the bits transmitted by the output units (see col. 8, lines 41-50 and col. 13, lines 37-41).

Regarding claim 4 Settle teaches a bit transmission circuit for transmitting a bit of predetermined data to an output unit (see col. 4, lines 6-11).

Regarding claim 5 Settle teaches transmitting two bits received from two different input units to two different output units separately (see col. 3, lines 9-12 and FIG. 7).

Regarding claim 6 Settle teaches a bus connected between the processor and the format converting circuit for transmitting the data between the processor and the format converting circuit (see col. 7, lines 57-61 and FIG. 6).

Regarding claim 7 Settle teaches a transmission circuit of a digital communication system that receives input data at a first rate and according to the input data generating output data at a second rate (see col. 1, lines 7-10 and col. 8, lines 41-44). Settle teaches a processor for controlling operations of the transmission circuit, the processor capable of accepting the input data and generating corresponding first data having a plurality of bits (see col. 8, lines 41-50 and col. 13, lines 37-41). Settle teaches a format converting circuit electrically connected to the processor for generating second data according to the first data and a converting control signal from the processor, and transmitting the second data to the processor (see col. 8, lines 41-50 and FIG. 7). Settle teaches wherein the processor generates an output signal at the second rate according to the second data (see col. 4, lines 6-11). Settle does not specifically teach a rate adaptation layer. Settle does teach an adaptation field (see col. 9, lines 46-47). Hong teaches a rate adaptation layer (see col. 6, lines 20-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device adapt to include realizing a rate adaptation layer because the combination would allow for improved output quality.

Regarding claim 8 Settle teaches a plurality of input units each for receiving on bit of the first data and a plurality of output units each for outputting one bit of the second data after receiving the bit (see col. 8, lines 39-44 and FIG. 7). Settle teaches a bit control circuit

electrically connected between the input units and the output units for generating bits outputted by the output units according to bits received from the input units (see col. 8, lines 41-50, col. 13, lines 37-41, and FIG. 7). Settle teaches transmitting a bit received by an input unit to an output unit without having the bit passing through other input and output units (see col. 8, lines 39-44). Settle does not specifically teach a number of bits between the bit received by the input unit and a most significant bit of the first data being different from a number of bits between the bit outputted by the output unit and a most significant bit of the second data. Hong teaches a number of bits between the bit received by the input unit and a most significant bit of the first data being different from a number of bits between the bit outputted by the output unit and a most significant bit of the second data (see col. 4, lines 26-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device adapt to include a number of bits between the bit received by the input unit and a most significant bit of the first data being different from a number of bits between the bit outputted by the output unit and a most significant bit of the second data because it would allow for Settle to achieve improved output quality in his system that converts data from different input sources and different formats to form a bit-stream for output in a selected output format.

Regarding claim 9 Settle and Hong teach a device as recited in claim 2 and is rejected given the same reasoning as above.

Regarding claim 10 Settle and Hong teach a device as recited in claim 6 and is rejected given the same reasoning as above.

Regarding claim 11 Settle and Hong teach a device as recited in claim 3 and is rejected given the same reasoning as above.

Regarding claim 12 Settle and Hong teach a device as recited in claim 4 and is rejected given the same reasoning as above.

Regarding claim 13 Settle and Hong teach a device as recited in claim 5 and is rejected given the same reasoning as above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wesler U.S Patent No. 5,850,389 discloses a high speed circular data bus system.

Bergenwall et al. U.S. Patent No. 6,996,079 discloses handover and interworking in radio system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon J. Miller whose telephone number is 571-272-7869. The examiner can normally be reached on Mon.-Fri. 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, George Eng can be reached on 571-272-7495. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

January 4, 2007

GEORGE ENG
SUPERVISORY PATENT EXAMINER